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# Remote Automatic Multipurpose Station

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TECHNICAL SUMMARY

During the past report period the LORAMS design has been updated and a second station has been completed to be installed near NARL at Barrow. This station will serve as the environmental test bed and will provide an additional signal for propagation monitoring.

A data logging receiving stystem has been designed and fabricated which will allow the data quality to be assessed.

A 10,240-bit digital recirculating memory has been fabricated and installed in the second LORAMS station.

TECHNICAL RESULTS

LORAMS Station #2

A block diagram of the second LORAMS station is shown in Figure 1. The signals from the sensors are conditioned to a $\pm$ 5v full scale level and then multiplexed to a 10-bit A/D converter. Once an hour, the sensors are sampled and entered into the recirculating memory. In the test system, five inputs will be used and only five bits of the A/D converter will be used thus 50 bits will be entered each hour. The memory will be discussed in more detail later on. The output of the memory is a trilevel signal in which a one is represented by a positive level and a zero by a negative level. This system of modulation allows a clock signal to be easily recovered at the receiving end.

The memory output causes the temperature compensated, voltage controlled crystal oscillator (TCVXO) to be deviated $\pm$ 85 Hz from its center frequency of 6.221850 MHz. The stability of the oscillator is $1 \times 10^{-6}$ thus the worst case frequency error is 6 Hz. The TCVXO drives directly a broadband 100 watt power amplifier. The filter and antenna tuner attenuate the harmonics and match the transmitter output to the DDRR antenna.

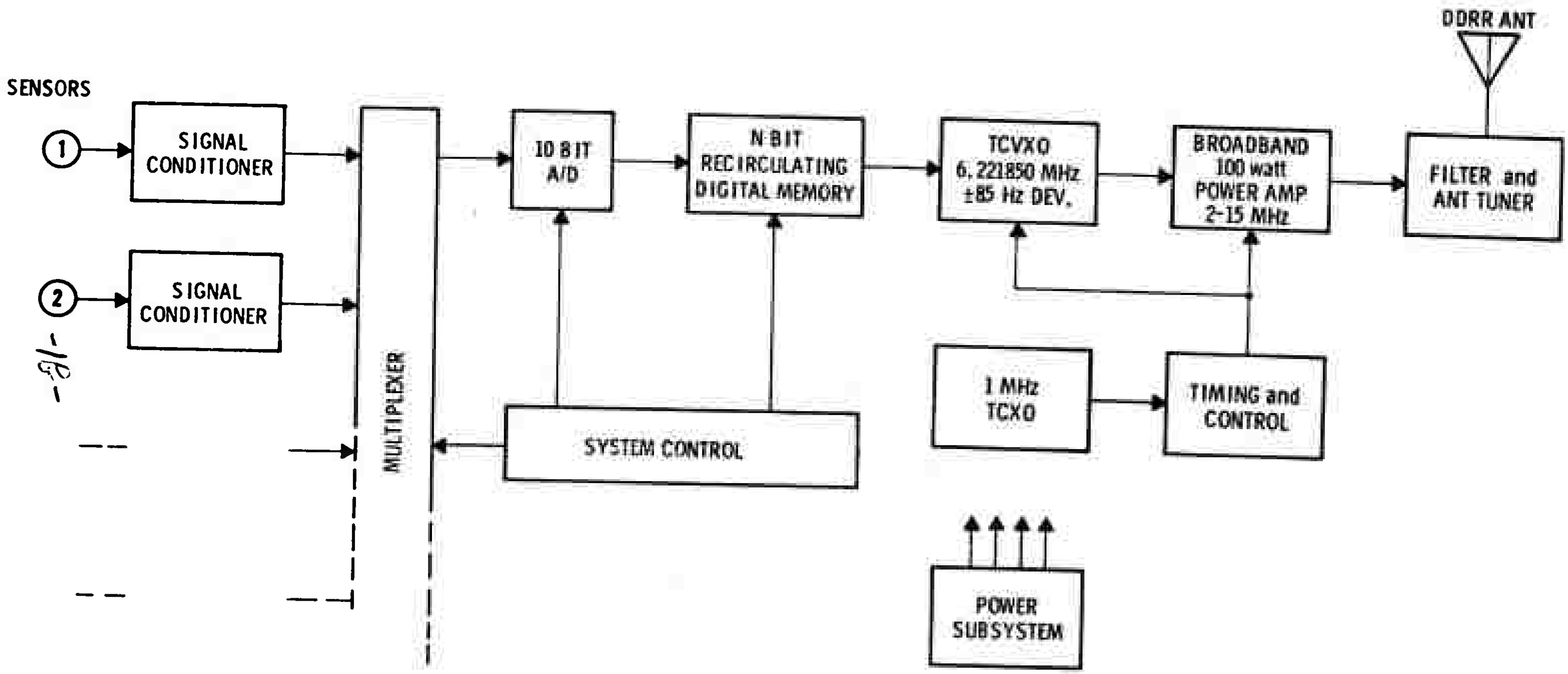


Figure 1 LORAMS System Block Diagram

The transmit cycle is controlled by the timing and control electronics which provides selectable turn-on cycle times of 2, 3, 4, 6, 12 or 24 hours and selectable transmission times of 2 to 10 minutes in one minute steps.

The 1 MHz TCVXO which drives the timing and control electronics has an accuracy of $5x10^{-7}$ therefore, the turn-on accuracy should be within one minute over a one-year period.

## Power Supply

A power supply consisting of an 8-watt TE cell and six lead acid batteries will be used for LORAMS #2.

## Recirculating Memory

The memory for LORAMS stores the output of an A/D converter at one hour intervals. The storage capacity is 10,240 bits which provides storage for 16 days. The A/D converter output is sampled at one hour intervals. The hourly sample will consist of five 5-bit words, four for 1/3 octave outputs and one for wind speed.

The memory consists of dynamic shift registers, timing circuits and associated control circuits. Monolithic Memories MM2404 shift registers are used. They provide 1024 bits of storage in a TO-99 package. The shift registers continually recycle and a new 25-bit data word is entered at one hour intervals. Each 24 hours a reference data group is entered into storage along with two 5-bit words giving the station number and the day number. Thus, the output of the memory is a serial string of 5 bit data words with a reference data group and the station number and day number inserted every 24 data words. When the memory is completely filled, the oldest data will be discarded as new data is entered.

The timing system provides clock pulses for the shift registers, one-hour timing signals to initiate the recording cycle, 24-hour timing signals to initiate the reference data group and a counter to count days for the daily reference recording.

The reference data group consists of a string of ten zeros and ten ones. The probability of getting two minimum readings followed by two maximum readings is very low and, thus, the reference group is unlikely to occur in the recorded data.

Data Logging Subsystem

The output of the receiver consists of an 850 Hz signal which is shifted $\pm 85$ Hz. This signal is fed into the data logger which demodulates the signal and provides punched paper tape as an output. The paper tape can be fed into a teletype machine or a computer for data recovery. A block diagram of the data logger is shown in Figure 2.

The receiver or recorder output is connected to a FSK data modem which demodulates the tones into a TTL compatible bit stream. A sync clock is also generated by the modem.

Data are loaded in serial, bit by bit, into a 30-bit shift register which has parallel outputs. Whenever the synchronizing words are contained in the first two word registers, a pulse is generated which resets the clock divider network. This causes the clock/10 and clock/2 signals to be properly synchronized with the data. Whenever a clock/10 occurs, data are transferred from the third input register to a 10-bit latch. Ten bit data words from the latch are then converted into 4-digit BCD codes. Ten bit identification words are also converted into 4-digit BCD codes, 2 digits indicating day numbers and 2 digits indicating buoy identification. The sync pulse controls the conversion of either type words. After the conversion takes place, the BCD words are transferred in parallel to a 5-character register. These characters, in ASCII format, are shifted at the clock/2 rate (bits in parallel). A parity generator controls the eighth bit before data are entered into the punch.

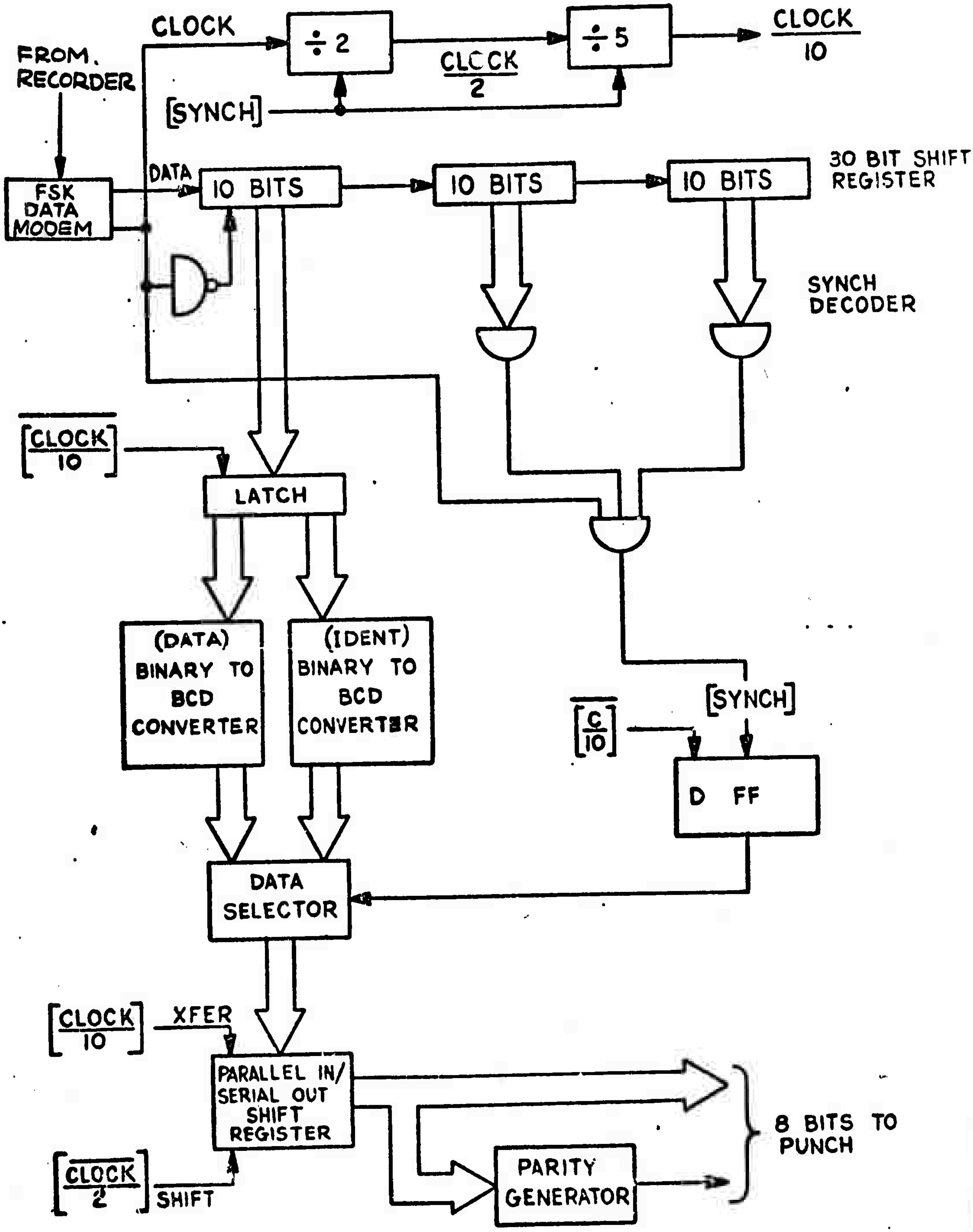


FIGURE 2. DATA LOGGING SUBSYSTEM

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## FUTURE WORK

The second LORAMS station will be installed in the vicinity of NARL, Barrow to provide a test bed for long term evaluation. A one-year supply of propane will be installed and provisions will be made for periodic monitoring.

A proposal will be prepared for Phase III.

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